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Polymer Electrolyte-Gated Organic Field-Effect Transistors: Low-Voltage, High-Current Switches for Organic Electronics and Testbeds for Probing Electrical Transport at High Charge Carrier Density

Matthew J. Panzer and C. Daniel Frisbie*

Contribution from the Department of Chemical Engineering & Materials Science, University of Minnesota, 421 Washington Ave S.E., Minneapolis, Minnesota 55455

Received February 7, 2007; E-mail: frisbie@cems.umn.edu

Abstract: We report the fabrication and extensive characterization of solid polymer electrolyte-gated organic field-effect transistors (PEG-FETs) in which a polyethylene oxide (PEO) film containing a dissolved Li salt is used to modulate the hole conductivity of a polymer semiconductor. The large capacitance (~10 μF/cm^2) of the solution-processed polymer electrolyte gate dielectric facilitates polymer semiconductor conductivities on the order of 10^3 S/cm at low gate voltages (<3 V). In PEG-FETs based on regioregular poly(3-hexylthiophene), gate-induced hole densities were 2×10^{14} charges/cm^2 with mobilities >3 cm^2/V·s. PEG-FETs fabricated with gate electrodes either aligned or intentionally nonaligned to the channel exhibited dramatically different electrical behavior when tested in vacuum or in air. Large differences in ionic diffusivity can explain the dominance of either electrostatic charging (in vacuum) or bulk electrochemical doping (in air) as the device operational mechanism. The use of a larger anion in the polymer electrolyte, bis(trifluoromethanesulfonyl)imide (TFSI$^-$), yielded transistors that showed clear current saturation and square law behavior in the output characteristics, which also points to electrostatic (field-effect) charging. In addition, negative transconductances were observed using the PEO/LiTFSI electrolyte for all three polymer semiconductors at gate voltages larger than −3 V. Bias stress measurements performed with PEO/LiTFSI-gated bottom contact PEG-FETs showed that polymer semiconductors can sustain high ON currents for greater than 10 min without large losses in conductance. Collectively, the results indicate that PEG-FETs may serve as useful devices for high-current/low-voltage applications and as testbeds for probing electrical transport in polymer semiconductors at high charge density.

Introduction

Recently, we and others have demonstrated that solid polymer electrolyte films, deposited from solution, can function as ultrahigh-capacitance gate dielectrics in organic field-effect transistors (OFETs).[1−12] The high capacitance of polymer electrolytes is afforded by mobile ions that can move to form electric double layers in an OFET structure. Capacitances exceeding 10 μF/cm^2 can be obtained, a value far larger than what is typically achieved with SiO_2 or polymer dielectrics (~10 nF/cm^2). The benefits of large capacitance are (i) much higher output currents at a given applied gate voltage and (ii) much lower operating gate voltages; both are a direct consequence of the large two-dimensional charge density that can be induced in the transistor channel by means of the high capacitance. Other high-capacitance, solution-processable gate dielectrics have been reported recently,[13−17] though so far none have capacitances that match values achievable with a solid polymer electrolyte. A disadvantage of solid polymer electrolytes for transistor applications is that switching speeds are limited by ion diffusivity within the electrolyte. However, switching speeds of a few hundred hertz are probably attainable, which is high enough for specific applications. It is noteworthy that electrolytes were used to gate conventional semiconductors as early as 1969,[18]

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and there have been extensive studies of inorganic semiconductor-based ion-sensitive field-effect transistors (ISFETs)[19−24] as well as semiconducting polymer-based electrochemical transistors[25−31] and ion sensors[32−33] in the last 30 years.

In this paper, we expand substantially on our earlier reports[9−12] and demonstrate that the polymer electrolyte system consisting of polyethylene oxide (PEO) plus a lithium salt can be used as the gate insulator in transistors employing a variety of polymer semiconductor films. Specifically, we show here that (i) solid polymer electrolytes based on PEO can be used to gate OFETs composed of three solution-processable polymer semiconductors, enabling high-output currents at low gate voltages; (ii) the results are general in that we can change the polymer semiconductor and the dissolved ions in the electrolyte to obtain qualitatively similar results; (iii) the conductance maximum previously reported[10−12] is also a generally observable phenomenon for all three polymer semiconductors, independent of the specific salt used; (iv) the induced charge density is substantial ($\sim 2 \times 10^{14}$ charges/cm^2 or ~ 30 μC/cm^2) and comparable for all polymer semiconductor systems examined; (v) quantitatively, there are important differences in the current−voltage characteristics between polymer electrolyte-gated OFETs (PEG-FETs) based on various semiconductors, yet the charge mobilities can be exceptionally large; thus there is nothing about the polymer electrolyte/semiconductor interface that precludes high mobilities; (vi) electrostatic charging (as opposed to electrochemical doping) can be the dominant operating mechanism in PEG-FETs under vacuum conditions; and (vii) bias stress effects can be small for PEG-FETs and are dependent on the polymer semiconductor employed. A schematic of the PEG-FET and an optical image of a completed device are displayed in Figure 1.

A key point of the current paper is the mechanism of transistor action in PEG-FETs. In particular, an important distinction can be made between *charging via the field-effect* (as occurs in conventional metal-oxide-semiconductor field-effect transistors, MOSFETs) and *electrochemical doping* operational modes.[34] The critical difference between these two mechanisms is the permeability of the semiconductor layer to the ions in the polymer electrolyte, Figure 2. In an electrochemical transistor,[25−31] ions migrate into the semiconductor to stabilize charges in the polymer semiconductor backbone; this constitutes an electrochemical reaction, or doping process, which increases the film conductivity. On the other hand, if ions do not penetrate into the semiconductor during OFET operation, current modulation is achieved by the electrostatic induction of charge carriers in the semiconductor in response to the high electric field at the polymer semiconductor/polymer electrolyte interface (i.e., the "field-effect" is operative). In this case, an electric double layer is formed at the polymer semiconductor/polymer electrolyte interface, Figure 2. These two scenarios represent limiting cases for the degree of ion migration into the polymer semiconductor, and a combination of the two mechanisms has also been used to explain OFET operation with an electrolyte gate.[8] Here, we present experimental evidence demonstrating that PEG-FETs can be operated via the field-effect under vacuum conditions,

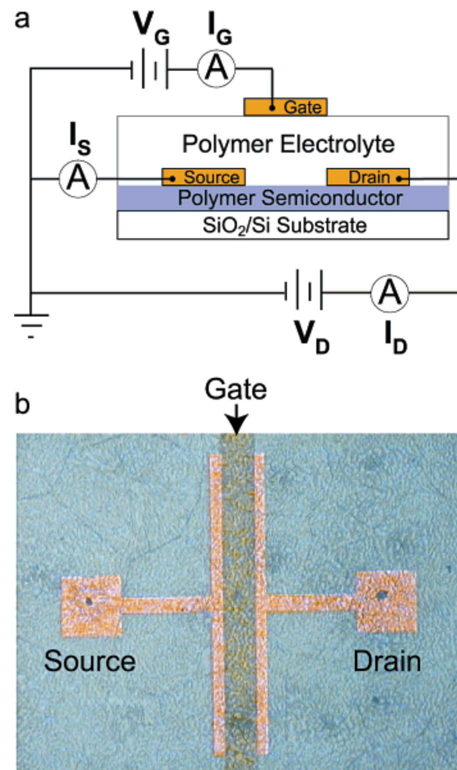

Figure 1. (a) Polymer electrolyte-gated organic field-effect transistor (PEG-FET) schematic in cross-section (not drawn to scale). Source (I_S), drain (I_D), and gate (I_G) currents were measured simultaneously while applying the source−gate (V_G) and source−drain (V_D) voltages. (b) Optical image of a completed PEG-FET (top view); the source−drain separation (channel length) is 200 μm, and the channel width is 2000 μm.

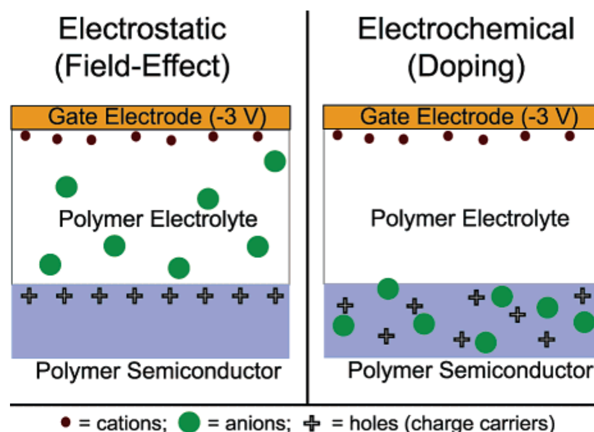

Figure 2. Schematic cross-sections of a portion of a PEG-FET channel showing the key difference in the extent of ion penetration between (a) electrostatic charging and (b) electrochemical doping as possible operating mechanisms.

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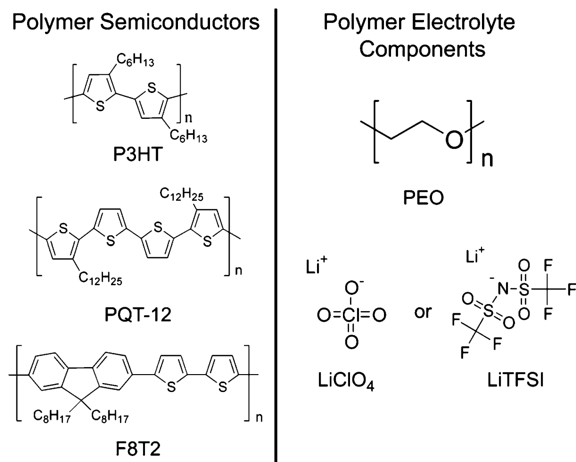

Figure 3. Molecular structures of the polymer semiconductors (left) and polymer electrolyte materials (right) utilized in this work.

distinguishing our devices from those that depend on electrochemical reaction to increase polymer semiconductor conductivity.

The difference between electrostatic and electrochemical charging mechanisms is potentially important to transistor performance, as in the former case intermolecular chain packing in the semiconductor is not disrupted, whereas this is not the situation with electrochemical doping. It is generally accepted that crystalline packing can result in higher carrier mobility. Thus, electrostatic charging of semicrystalline polymer semiconductors may result in higher mobilities than can be obtained with electrochemically doped polymer semiconductors.

Overall, our results point to the potential for PEG-FETs to be used both as low-voltage, high-output current switches employing solution-processable materials and also as experimental platforms for studying charge transport at high two-dimensional (2D) carrier densities. The ability to utilize various polymer semiconductors and different polymer electrolyte components highlights the versatility of these devices for fundamental research and for the development of new applications within the field of organic electronics.

Experimental Section

The molecular structures of the three polymer semiconductors and the polymer electrolyte constituents employed in this study are shown in Figure 3.

Poly(3-hexylthiophene) (P3HT) was purchased from Aldrich; poly-(3,3‴-didodecylquaterthiophene) (PQT-12) and poly(9,9′-dioctylfluorene-*co*-bithiophene) (F8T2) were purchased from American Dye Source. Both P3HT and PQT-12 were purified by successive Soxhlet extractions,[35] while F8T2 was used as received. Dichlorobenzene solutions (3 mg/mL) of P3HT and PQT-12, along with a 4.4 mg/mL solution of F8T2 in mixed xylenes, were prepared in ambient conditions. Polymer electrolyte solutions were made by dissolution of polyethylene oxide (PEO) (Alfa Aesar, 100 000 MW) in acetonitrile at a concentration of 3−6% by weight, simultaneously with enough of either ionic salt (lithium perchlorate ($LiClO_4$, Fluka) or lithium bis(trifluoromethanesulfonyl)imide (LiTFSI, 3 M)) added to yield a Li^+:ether oxygen molar ratio of 1:16. The polymer electrolyte solutions were prepared in ambient conditions and filtered through 0.45 μm syringe filters.

PEG-FETs were fabricated in a manner described previously.[12] Spin-coating was used to form the polymer semiconductor layer, followed by thermal evaporation of metal electrodes and drop-casting of the polymer electrolyte dielectric layer. Typical film thicknesses for the semiconductor and polymer electrolyte layers were 20 nm and 3 μm, respectively. It should be noted that a crystalline PEO morphology was observed for both PEO/$LiClO_4$ (Figure 1b) and PEO/LiTFSI (Supporting Information) films at the salt concentration used in this study.

Current−voltage ($I-V$) characteristics were measured using a combination of two Keithley 236 source-measure units and a Keithley 6517 electrometer connected to a Desert Cryogenics vacuum probe station. Bias stress measurements were performed by applying fixed source−drain (V_D) and source−gate (V_G) voltages and continuously measuring the source−drain current. In this work, we examined differences in PEG-FET operation when electrical measurements were carried out either in vacuum ($\sim 10^{-6}$ Torr) or in air (probe station open to ambient laboratory atmosphere). Some devices were also tested under a nitrogen atmosphere, obtained by first evacuating the probe station chamber to a pressure below 10^{-5} Torr, then venting it with dry N_2 to a pressure of 760 Torr. All electrical measurements were performed in the dark at room temperature (300 K).

Results and Discussion

1. PEG-FET Electrical Characterization and Analysis. The upper panels of Figure 4 show the I_D-V_G characteristics of PEG-FETs based on P3HT, PQT-12, and F8T2. Differences in the curves between the three semiconductors are evident. First, the P3HT device (Figure 4a) shows the largest transconductance (dI_D/dV_G) of the three ($>10^{-3}$ S), but also exhibits a doubly inflected curve shape on the forward trace, which is not observed on the reverse sweep. The PQT-12 I_D-V_G characteristic (Figure 4b) is the most ideal, displaying only a small amount of hysteresis between the forward and reverse traces. In the case of F8T2 (Figure 4c), a large amount of hysteresis and a higher OFF current level following the reverse sweep both indicate a substantial amount of charge-trapping.

It should be noted that the P3HT PEG-FET drain current measured at a gate voltage of −3 V ($\sim 10^{-3}$ A) was obtained with a transistor channel aspect ratio (width:length) of only 10:1, which corresponds to a channel conductivity of 10^3 S/cm (10 kΩ/sq sheet resistance), assuming a channel thickness of 1 nm (a characteristic value for field-effect charging). The current density in the P3HT channel reached 5×10^4 A/cm^2 at its maximum value. This magnitude of conductivity is on par with that observed in metallic polymer samples.[3] Indeed, we have shown previously for P3HT PEG-FETs that the temperature dependence of the channel resistance is quite weak at high carrier density, consistent with the transition to metallic behavior.[12] Temperature-dependent studies of PQT-12 and F8T2 transistors will be the subject of future work. It is also noteworthy that the transconductance of P3HT devices ($>10^{-3}$ S) greatly exceeds that typically observed in hydrogenated amorphous silicon transistors, which exhibit transconductances of $\sim 10^{-6}$ S and channel conductivities of ~ 10 S/cm (1 MΩ/sq sheet resistance).[36]

The PEG-FET I_G-V_G data are shown in the lower panels of Figure 4. Here, too, the PQT-12 data (Figure 4b) are the most straightforward, displaying negative and positive peaks corresponding to the injection and subsequent removal of charge carriers (holes) during the forward and reverse sweeps, respectively. The F8T2 I_G-V_G curve (Figure 4c) also shows distinct charge injection and removal steps, although a higher amount of electronic leakage current (source/drain to gate) likely

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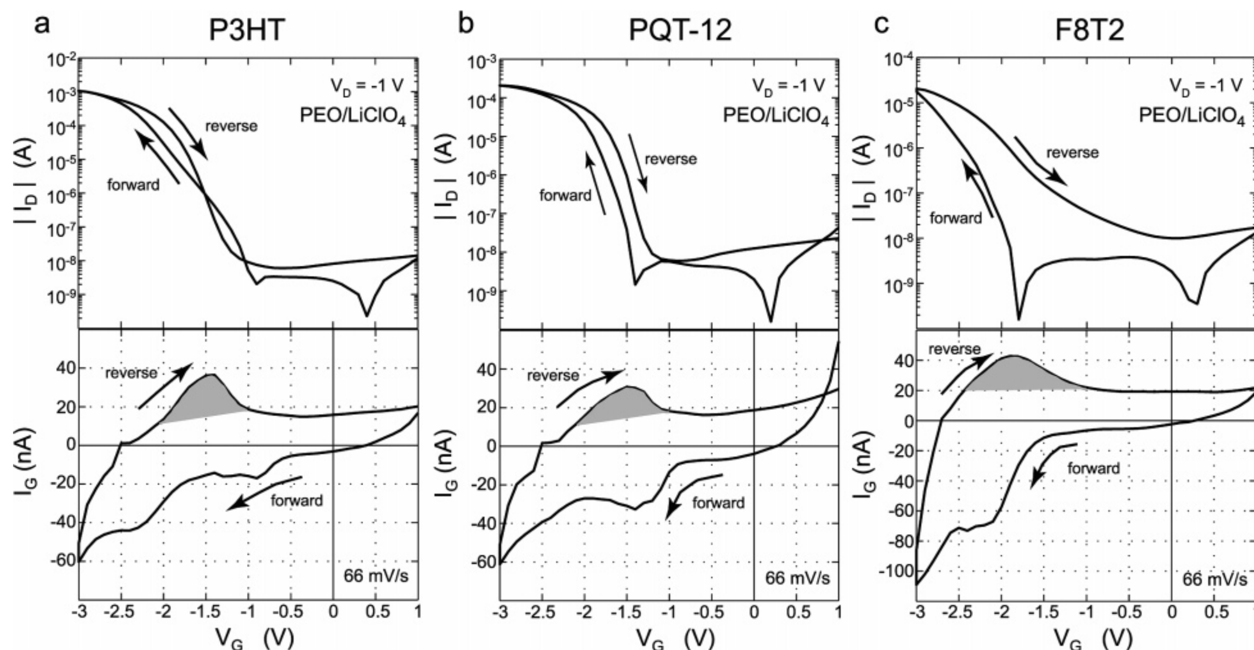

Figure 4. I_D-V_G and I_G-V_G characteristics measured simultaneously for PEO/LiClO$_4$-gated (a) P3HT, (b) PQT-12, and (c) F8T2 PEG-FETs in vacuum ($\sim 10^{-6}$ Torr). The gray shaded regions on the reverse sweeps of the I_G-V_G curves indicate the integrated peak areas used to calculate the total injected charge carrier (hole) densities in each semiconductor by the application of V_G up to -3 V. These 2D hole densities are 2.0×10^{14}, 1.5×10^{14}, and 2.5×10^{14} charges/cm^2 for a, b, and c, respectively. Sharp depressions in the I_D-V_G characteristics are an artifact of plotting the absolute value of I_D on a logarithmic scale. The gate voltage was swept at a rate of 66 mV/s.

obscured the precise onset of injection on the forward sweep. In contrast to the other two systems, the P3HT I_G-V_G data reflect an apparent "two-step injection" process during the forward sweep. First, a negative peak is observed around $V_G = -1$ V, corresponding to the first significant increase in I_D. Following a region of lower transconductance (-1.3 V < V_G < -2 V) in the I_D-V_G characteristic, a second negative peak in the I_G-V_G curve occurred at $V_G = -2.3$ V. A possible explanation for this behavior is that holes encounter different HOMO band density of states distributions during charge injection and charge extraction in the P3HT devices. In addition, energy level distinctions between charging the crystalline and amorphous regions in P3HT may be responsible, although further work is needed to fully understand the origins and implications of this phenomenon.

Since polymer electrolyte capacitance is humidity-,[37] frequency,[37] and gate voltage-dependent,[10] we calculated the total injected 2D charge carrier density (Q') by integrating the displacement current versus time data, similar to the analysis of a cyclic voltammogram.[12] The shaded areas under the reverse sweeps of the I_G-V_G curves (Figure 4) correspond to hole densities of 2.0×10^{14}, 1.5×10^{14}, and 2.5×10^{14} charges/cm^2 (32, 24, and 40 μC/cm^2) for the P3HT, PQT-12, and F8T2 PEG-FETs, respectively. By subtracting a baseline of background charging current from the I_G-V_G data during integration, we have attempted to obtain conservative values of the injected charge density (uncertainty in the integrated values is approximately $\pm$ 20%). In addition, while the integrated areas of the forward and reverse sweep I_G-V_G peaks should be approximately equal (Figure 4b) if all of the injected holes are subsequently removed, any irreversible trapping of charges in the semiconductor will lead to a *smaller* integrated peak area on the reverse sweep, which is a second means of ensuring that the calculated Q' values are indeed conservative. Because the observed gate current (I_G) is composed of the sum of *ionic* displacement current and *electronic* leakage (i.e., source/drain to gate), the magnitude of electronic leakage must be considerably less than the ionic displacement current in order to perform an accurate charge integration. We determine the magnitude of electronic leakage by simultaneously measuring both the source (I_S) and drain (I_D) currents flowing to a common ground (Figure 1a) and comparing the two; nearly ideal devices (with little electronic leakage) display I_S equal in value to I_D when the transistor is ON.

Using the integrated charge density values and the maximum I_D currents measured at $V_G = -3$ V from Figure 4, linear mobility values of 3.4, 0.9, and 0.04 cm^2/V·s were calculated for P3HT, PQT-12, and F8T2, respectively. Compared to the mobilities normally obtained using as-spun, unoptimized films of these semiconductor materials,[38-40] the PEG-FET values are quite large. It is possible that the very large induced charge densities effectively fill a higher fraction (if not all) of the charge carrier traps, leading to higher hole mobilities than are usually observed. It is worth emphasizing that the key advantage of PEG-FETs compared with other low-voltage transistors fabricated with traditional dielectrics is the achievement of very high charge densities *concomitant with* the preservation of high carrier mobility. This combination is evidenced by the extremely large I_D values obtained (>1 mA, Figure 4a) at low gate voltage with a transistor channel aspect ratio of 10:1.

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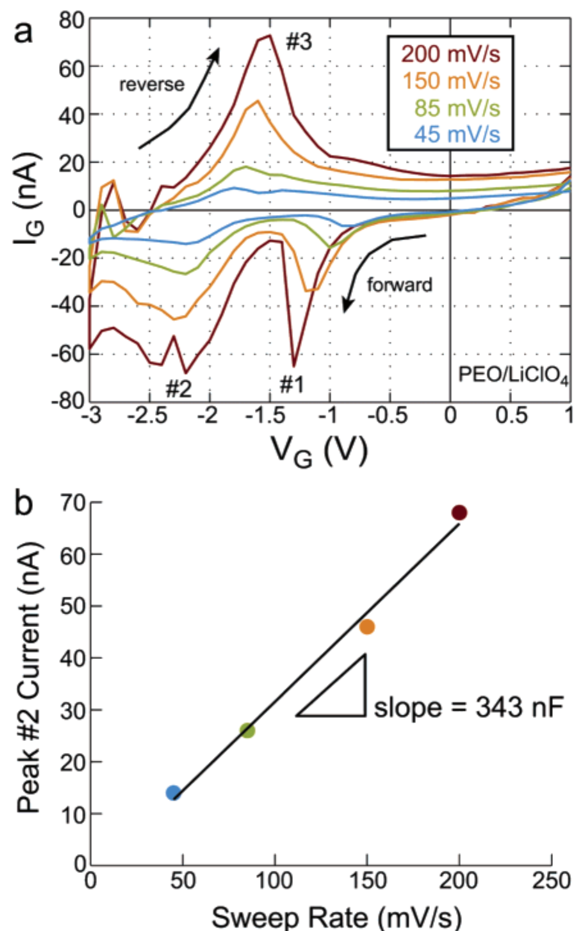

Figure 5. (a) I_G-V_G data measured for a PEO/$LiClO_4$-gated P3HT transistor at four different V_G sweep rates in vacuum. (b) Plot of peak current for the second peak of the I_G-V_G forward sweeps (#2) versus sweep rate, showing a linear trend. The gated semiconductor area was 0.006 cm^2.

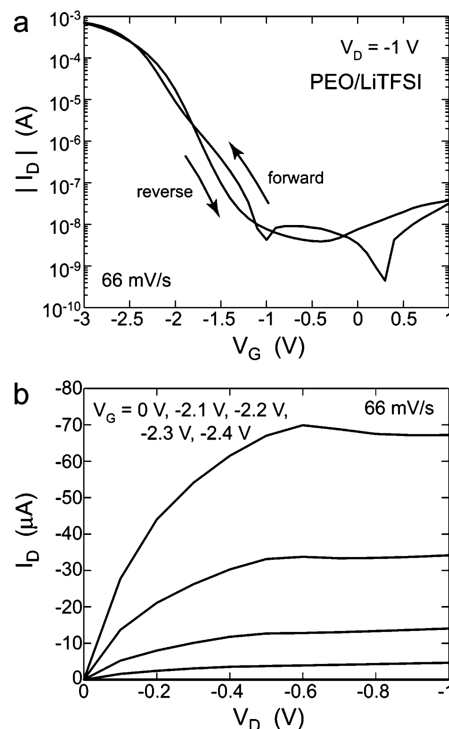

Figure 6. (a) I_D-V_G characteristic of a PEO/LiTFSI-gated P3HT transistor measured in vacuum. (b) I_D-V_D curves for five different applied gate voltages: $V_G = 0$, −2.1, −2.2, −2.3, and −2.4 V (forward sweeps shown), showing clear saturation behavior and a square-law dependence of the saturation currents on V_G.

Using a polymer electrolyte-gated P3HT device that exhibited very low leakage current, we measured I_G-V_G data at several gate voltage sweep rates (Figure 5). The unique I_G-V_G features observed for P3HT PEG-FETs, the aforementioned presence of two well-defined peaks on the forward sweep and only one peak on the reverse sweep, are clearly visible in Figure 5a. The integrated charge densities were 6.1×10^{13}, 1.3×10^{14}, and 2.1×10^{14} charges/cm^2 for peaks #1−3, respectively. All three peak current values scaled linearly with the sweep rate with approximately the same slope, which has units of capacitance (data for peak #2 are shown in Figure 5b). Linear scaling of the displacement current with the voltage sweep rate is expected for capacitive charging; however, we note that any significant ion diffusion limitations would lead to nonlinear scaling.[41] As for the general appearance of peaks in the I_G-V_G data, we suggest that given the very large capacitance of the polymer electrolyte, it is possible that we are able to completely sweep through the narrow bandwidth[42] of the semiconductor HOMO band with only a few volts and thereby observe an I_G-V_G characteristic similar to that seen in an adsorbed monolayer cyclic voltammetry experiment.[41]

2. Operating Mechanism. We carried out two principal experiments to investigate the switching mechanism in PEG-FETs, in particular to establish the role of electrostatic charging via the field-effect versus electrochemical doping. First, we investigated the role of the anion. In order to determine whether changing the electrolyte anion would affect device operation, we fabricated PEG-FETs with PEO/LiTFSI as the solid polymer electrolyte.

Figure 6 shows both the I_D-V_G (Figure 6a) and I_D-V_D (Figure 6b) characteristics of a PEO/LiTFSI-gated P3HT transistor tested in vacuum. The P3HT I_D-V_G characteristic of the PEO/LiTFSI device is comparable to that of the PEO/$LiClO_4$ PEG-FET (Figure 4a). Similar performance between the two P3HT devices using different anion-based polymer electrolytes suggests a field-effect charging mechanism, because the larger volume of a single $TFSI^-$ anion (147 Å^3, approximately 3 times that of ClO_4^-)[43] would be expected to cause greater hysteresis in the I_D-V_G data if an electrochemical doping process (requiring the motion of anions into the bulk of the semiconductor) was dominant. Large amounts of current leakage made the measurement of I_G-V_G characteristics for the LiTFSI devices difficult, although the general shape of the I_G-V_G curve was similar to that observed for $LiClO_4$-gated transistors (see Supporting Information). A higher degree of leak in the LiTFSI-gated PEG-FETs may be ascribed to a known plasticizing effect that the $TFSI^-$ anion has on PEO,[44] which likely weakened its mechanical/thermal stability and resulted in a greater penetration of gold atoms during the gate electrode deposition process. The output characteristics of the PEO/LiTFSI devices (Figure 6b)

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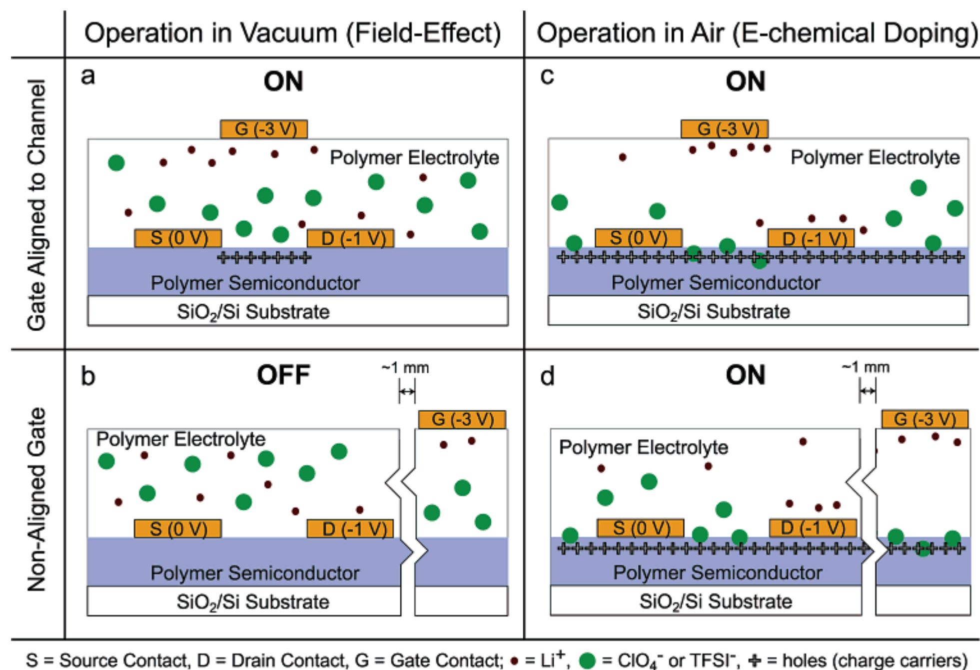

Figure 7. Illustrations showing the proposed operating mechanisms for PEG-FETs operated in vacuum ($\sim 10^{-6}$ Torr) conditions (a and b), where electrostatic induction (i.e., the field-effect) is dominant; for those devices tested in ambient atmosphere (c and d), electrochemical doping occurs.

are of great importance because they show clear saturation behavior and obey the well-known field-effect transistor square-law behavior.[45] This result also suggests a field-effect charging mechanism in PEG-FETs, because current saturation (caused by channel pinch-off) is an indicator of the largely 2D nature of charge transport in a traditional field-effect transistor (MOSFET) and not of 3D, bulk chemical doping. In general, clear current saturation is *not* typically observed for electrochemical transistors where 3D doping occurs.[5,27,46] One recent exception, however, is a depletion mode transistor[47,48] that utilized poly-(3,4-ethylenedioxythiophene):poly(styrene sulfonate) (PEDOT:PSS) as both the semiconductor and source/drain material, although comparison of that device to the PEG-FET geometry reported here is not straightforward. Note that we cannot strictly rule out the possibility of fast, reversible anion incorporation in a *very thin* layer of the polymer semiconductor next to the polymer electrolyte, which would give results approximately equivalent to those expected in a field-effect device. However, the bulkiness of the $TFSI^-$ anion and our previous results on polymer electrolyte-gated organic single crystals (which have a nonporous, compact crystal structure) strongly argue against this possibility.[11]

In order to further support the hypothesis of electrostatic charging via the field-effect, we fabricated devices where a gate electrode was *not aligned* to the source−drain channel, but instead was located approximately 1 mm away. We then electrically characterized the aligned- and nonaligned gate transistors both in vacuum ($\sim 10^{-6}$ Torr) and in the ambient laboratory atmosphere. Significant differences were observed between vacuum and ambient (air) operation. While the aligned-gate transistors showed a large increase in source−drain conductivity with the application of a negative gate voltage (i.e., they turned on) when operated both in vacuum and in air, devices with a nonaligned gate showed *no turn on* when tested in vacuum, but, in contrast, they did turn on in air. Illustrations of these results and proposed operating mechanisms for the various cases are shown in Figure 7.

The difference in the operating mechanism between vacuum and ambient testing may be explained in terms of ionic mobility. Because PEO is hygroscopic, the conductivity of the PEO-based polymer electrolyte is greatly increased upon hydration[37] (residual solvent in the electrolyte layer would also increase ionic conductivity). Thus, when the electrolyte is exposed to air, anions have sufficient mobility to migrate from the PEO matrix *into* the polymer semiconductor and electrochemically oxidize it *no matter where* the gate electrode is placed (Figure 7c,d) on the *time scale* of our I_D-V_G sweeps. Polarization of the entire electrolyte volume (and subsequent doping of the whole polymer film) can occur, which is the well-known mechanism of solid-state cyclic voltammetry.[49] During the operation of our transistors in air, evidence for bulk electrochemical doping was observed in the form of an irreversible, visible color change in the semiconductor film that occurred over a large area (as viewed through the transparent polymer electrolyte), not just beneath the gate electrode (Supporting Information). No color change was observed during operation in vacuum.

In contrast, however, we believe that operating these transistors in vacuum dries out the PEO matrix and dramatically reduces both the cation and anion diffusivities (especially that of the larger anion). In this situation, bulk polarization of the solid polymer electrolyte does not occur rapidly; rather, only those ions directly underneath the gate electrode (primarily the smaller cations) are able to migrate significantly under the

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influence of the applied gate voltage (i.e., large electric field). Importantly, we believe that the lack of bulk electrolyte polarization *in vacuo* is due to a kinetic limitation, since the time scale of our transistor sweeps (~45 s OFF-to-ON) together with low ion diffusivity values do not allow for an equilibrium ion distribution to be achieved. Therefore, a vertical polarization beneath the gate electrode occurs *without* significant anion motion, and a 2D sheet of holes is able to rush into the semiconductor layer due to the extremely large electric field created at the polymer electrolyte−semiconductor interface (Figure 7a). The fact that electrostatic charging occurs directly beneath the gate electrode, as in standard OFET operation, explains why the nonaligned gate devices did not show any turn-on when tested in vacuum. That is, in vacuum the gate must be positioned over the channel to turn the transistor on. This is of course consistent with field-effect operation of traditional silicon MOSFETs. Note that similar results to in-vacuum measurements were obtained when the transistors were tested in a dry nitrogen atmosphere, emphasizing the role water plays in the operating mechanism of these devices.

The concept of ion mobility can also be used to contrast our nonaligned gate devices with those recently reported by the Berggren group,[2] where a polyanionic proton conductor was used to gate an OFET. In their report, testing the devices in humid air afforded a proton diffusivity large enough to turn on a nonaligned gate transistor due to bulk polarization of protons from the entire electrolyte volume. In spite of the facile *cation* polarization, the authors claimed that bulk electrochemical doping did not occur because the anions were covalently bound to the polymer electrolyte matrix and could not migrate into the semiconductor layer. This result supports our hypothesis that an electrostatic charging mechanism is operative in situations where *anion* diffusivity (for hole-conducting, or "p-channel" semiconductors) is very low.

Figure 8 shows the electrical characteristics of an I_D-V_G sweep for a *nonaligned* gate device tested in vacuum. While it is clear from Figure 8a that the transistor does not show any significant current modulation (turn-on) within $|V_G| < 3$ V, more striking is the stark difference between the I_G-V_G characteristic seen here (Figure 8b) and that of an aligned-gate transistor (Figures 4, 5a). By adding the values of the source and drain currents for the nonaligned gate device (this is equal to $I_S - I_D$ because I_D was measured with the opposite sign convention), it is revealed in Figure 8b that the gate current matches this sum almost exactly. Thus, the I_G-V_G characteristic for the nonaligned gate device tested in vacuum is due solely to electronic leakage from both the source and drain electrodes to the gate. The absence of any evidence of charge injection in the I_G-V_G data when the gate is not directly over the channel (in contrast to the distinctive peaks seen in the aligned gate PEG-FET I_G-V_G curves) is consistent with field-effect charging as the dominant mechanism in vacuum.

3. Negative Transconductance. Importantly, a quasi-reversible maximum in the I_D-V_G characteristic was also observed for PEO/LiTFSI-gated OFETs (Figure 9) based on all three polymer semiconductors. We have previously observed negative transconductance ($dI_D/dV_G < 0$) for PEO/$LiClO_4$-gated polymeric,[12] oligomeric,[10] and organic single-crystal semiconductors.[11] While the P3HT PEG-FET displayed the highest ON currents, the best reversibility (lowest hysteresis) of the negative

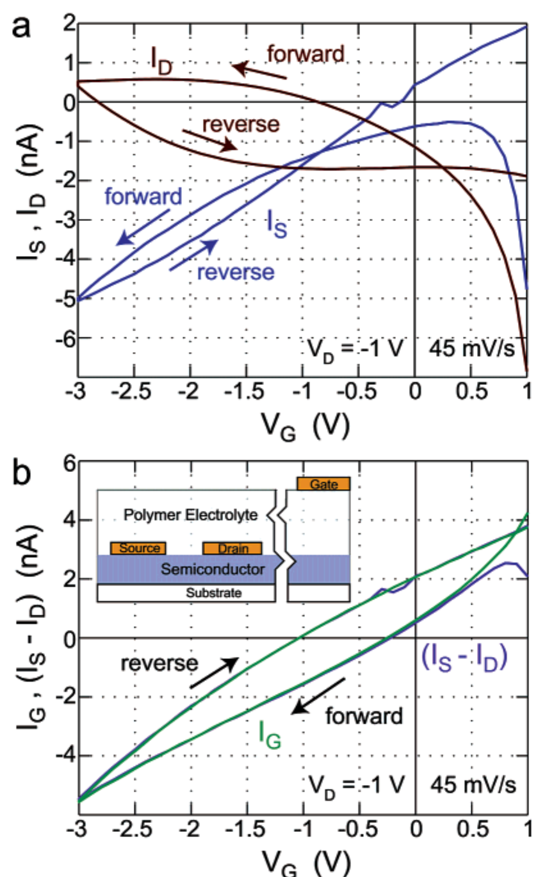

Figure 8. (a) Source (I_S) and drain (I_D) currents measured during an I_D-V_G sweep of a nonaligned gate PEO/$LiClO_4$-gated P3HT transistor tested in vacuum. (b) Gate current (I_G) and the sum of the source and drain currents ($I_S - I_D$) measured simultaneously for the same device (the current sign convention for I_D is opposite that of I_S). Inset shows a schematic of the nonaligned gate device (not drawn to scale).

transconductance behavior was observed for PQT-12 devices. Collectively, these results show that negative transconductance (or a peak in the I_D-V_G curve) is a general phenomenon, not limited only to the $LiClO_4$-based electrolyte devices.

As described earlier, the large capacitance of the polymer electrolyte allows induction of charge density levels well above those normally achieved in OFETs at low gate voltages, even approaching densities required to completely exhaust the HOMO band of electrons. In such a situation, it is possible that the achievement of large carrier densities in an ~1 nm thick semiconductor PEG-FET channel (2×10^{14} charges/cm^2 or $>10^{21}$ charges/cm^3) would lead to carrier−carrier interactions that could cause a decrease in semiconductor mobility (thus, in channel conductivity). Although we have presented evidence here that ions do not significantly penetrate into the semiconductor layer during vacuum operation, we cannot exclude the possibility that some degree of ion migration into the semiconductor layer might also lead to a decrease in the channel conductivity. A series of simplified energy band diagrams, shown in Figure 10, can be used to illustrate the "overcharging" of the HOMO band. At zero gate bias, the HOMO band is filled (and not aligned to the source Fermi level), so no source-to-drain current passes (point A in Figure 10). As the gate voltage is swept more negative, the positions of the LUMO and HOMO bands rise in energy, allowing mobile holes to sustain a source-to-drain current via a partially filled HOMO band (point B).

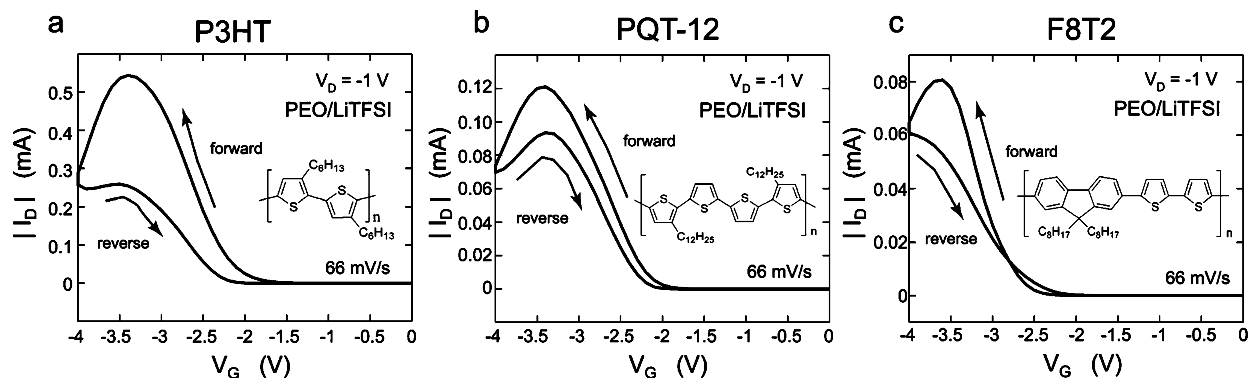

Figure 9. I_D-V_G characteristics displaying quasi-reversible conductivity maxima and negative transconductance for PEO/LiTFSI-gated (a) P3HT, (b) PQT-12, and (c) F8T2 PEG-FETs measured in vacuum. Insets show the molecular structures of each polymer semiconductor.

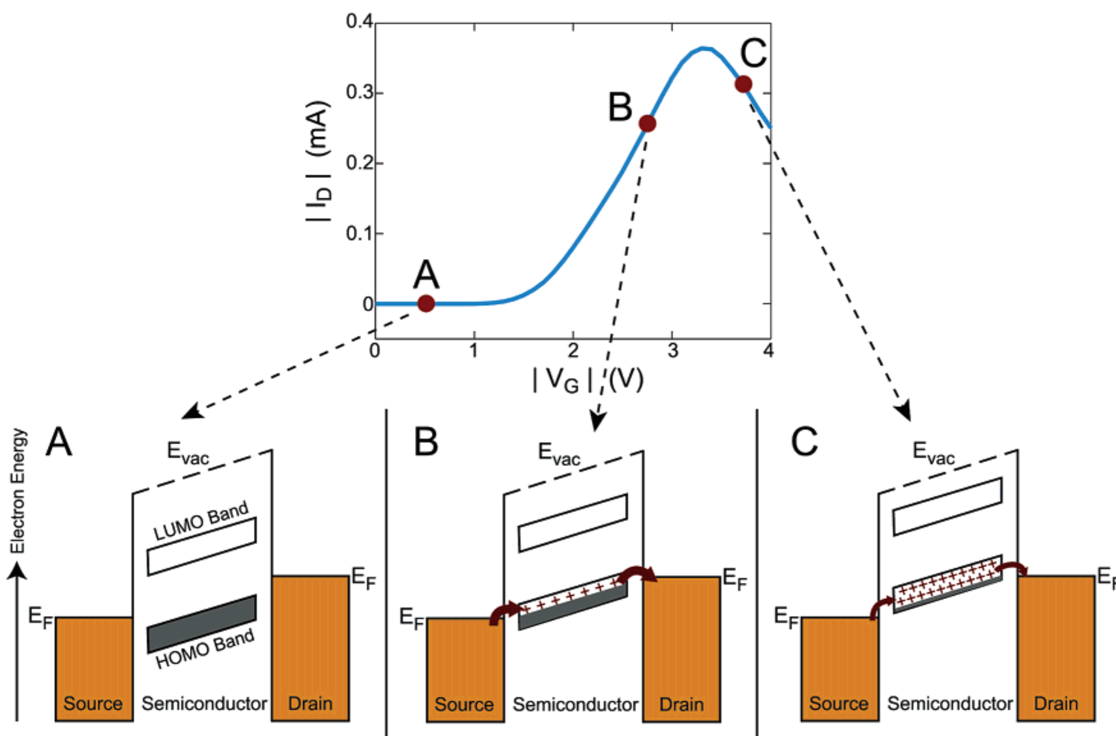

Figure 10. Sample I_D-V_G characteristic displaying a conductivity maximum and negative transconductance for a PEG-FET. Points A, B, and C correspond to transistor OFF, ON, and negative transconductance states, respectively. Simplified energy band diagrams indicate an offset in the source and drain Fermi energy levels (E_F) and the vacuum level (E_{vac}) due to an applied negative drain bias (relative to a grounded source). Source−drain current is due to the motion of holes (+) through a partially filled HOMO band (B); however, the mobility of these charge carriers could be reduced as the extent to which the HOMO band is filled with holes (emptied of electrons) approaches 100% (C).

When the gate voltage is large enough to virtually exhaust the HOMO band of electrons, hole−hole interactions lead to a decrease in the source−drain current and a negative transconductance (point C).

Calculated hole densities were $\sim 2 \times 10^{14}$ charges/cm^2 for our PEG-FETs at V_G = - 3 V; in comparison, the 2D density of thiophene rings at a P3HT-insulator interface has been estimated as 6.6×10^{14} rings/cm^2.[50] In order to more *precisely* determine the charge density value at which the conductivity peaks for a given semiconductor, further reduction of I_G-V_G leakage currents and the use of alternative charge measurement techniques (e.g., infrared absorption spectroscopy) are currently being explored.

4. Bias Stress Testing and Future Outlook. Finally, we have performed bias stress measurements on PEG-FETs in order to measure their robustness to continuous, high-current operation (current densities exceeding 5×10^4 A/cm^2). The best devices (i.e., those that showed the smallest bias stress) were PEO/LiTFSI-gated transistors with a bottom contact geometry. Bottom contacts were formed by thermal evaporation of gold source and drain electrodes onto the SiO_2/Si substrate prior to spin-coating the polymer semiconductor film; all other fabrication steps were the same. Figure 11 shows the bias stress curves for all three polymer semiconductors gated by PEO/LiTFSI with constant $V_G = -3$ V and $V_D = -1$ V applied.

As seen in Figure 11, PQT-12 exhibited the smallest loss in conductance, with I_D dropping by only 13% of its initial value (0.1 mA) after 10 min of continuously applied bias. Both P3HT and F8T2 displayed greater current losses, with conductance values falling by approximately 35% after 10 min of continuous stressing (initial currents of 0.45 and 0.038 mA for P3HT and

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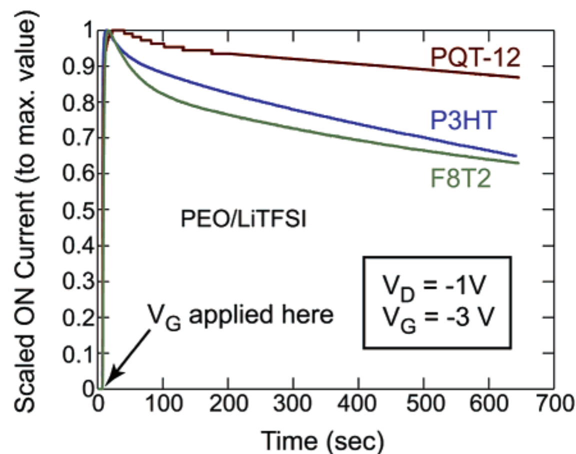

Figure 11. Normalized ON current (I_D) measured versus time (in vacuum) for a constant bias of $V_D = -1$ V and $V_G = -3$ V for bottom contact, PEO/LiTFSI-gated films of PQT-12, P3HT, and F8T2.

F8T2, respectively). Comparison of the turn-on voltage location (logarithmic increase in I_D) between I_D-V_G sweeps measured for the devices directly before and after the bias stress tests revealed almost no change in position. Thus, the small current loss due to continuous biasing may be explained by slow but reversible hole-trapping (leading to lower carrier mobility). Nevertheless, the relative stability of the high conductivities achieved at very high 2D charge carrier densities in these semiconducting polymers is encouraging.

While PEG-FETs are convenient for boosting transistor output current by obtaining high charge carrier densities from a solution-processable dielectric material, they do have a few drawbacks. The rough, polycrystalline morphology of the PEO/lithium salt film not only leads to increased gate leakage currents but also restricts one to building the gate/insulator stack on top of the semiconductor layer (the so-called "top gate" architecture). It would be desirable to be able to build the OFET from the bottom up, forming an ultrasmooth polymer electrolyte layer on the gate electrode *before* depositing the semiconductor layer, especially for the case of thermally evaporated polycrystalline semiconductor films. Plasticizing the PEO to prevent its crystallization (by increasing the LiTFSI concentration, for example) is one strategy we have explored; however, this results in a severe decrease in mechanical stability of the electrolyte film, complicating subsequent transistor fabrication steps.

Another limitation of using the polymer electrolyte in a "dry" form (under vacuum) is its low ionic conductivity. While we believe this may help prevent bulk electrochemical doping from occurring in the semiconductor layer on the time scale of our experiments, it also severely restricts the switching speed of PEG-FETs to a few hertz. Possible approaches to increasing electrolyte ionic conductivity include the following: increasing the salt concentration,[51] raising the operating temperature,[51] or using a gel electrolyte based on an ionic liquid.[52,53] The gel electrolyte strategy is particularly intriguing, as it may alleviate both the low ionic conductivity *and* the electrolyte roughness issues. These approaches are currently under investigation in our laboratory.

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The most promising polymer semiconductor studied here for use in future PEG-FETs is clearly PQT-12. Not only are the I_D-V_G and I_G-V_G characteristics for this polymer (Figure 4b) the cleanest, most reversible (Figure 9b), and most straightforward to interpret, but PQT-12 PEG-FETs also exhibited the highest stability to continuous bias stress (Figure 11). Output currents at −3 V applied to the gate for PQT-12 devices routinely approached 1 mA, yielding estimated linear mobility values on the order of 1 $cm^2/V{\cdot}s$. At this high level of performance, many potential applications of PEG-FETS, including flexible displays and sensors, can be imagined. Further, the utility of the PEG-FET as a test structure for measuring charge transport in organic semiconductors at very high carrier density has been demonstrated. There certainly remains room to improve the switching speed of these transistors, and further design and improvement of the solid polymer electrolyte layer are underway.

Conclusions

We have fabricated polymer electrolyte-gated P3HT, PQT-12, and F8T2 transistors with two different polymer electrolyte compositions: PEO/$LiClO_4$ and PEO/LiTFSI. Conservative integration of the transient gate current (I_G-V_G characteristics) indicated that it is possible to induce approximately 2×10^{14} holes/cm^2 with the application of −3 V to the gate electrode in these devices. The combination of large charge density values and strikingly high hole mobility values (up to 3.4 $cm^2/V{\cdot}s$ for P3HT) yielded very large source−drain currents (>1 mA) in low aspect ratio (10:1) PEG-FET channels, corresponding to conductivities of $\sim 10^3$ S/cm. Persuasive evidence was offered for 2D, electrostatic charging when the devices were tested in vacuum. Indications of a different operating mechanism, namely, bulk electrochemical doping, were observed upon testing in air. Vast differences between the ion mobility values in the PEO matrix under vacuum or in ambient conditions can explain the dominance of one operational mode over the other. Current saturation and square-law behavior in the I_D-V_D characteristics of a PEO/LiTFSI-gated OFET measured in vacuum also indicate the formation a 2D layer of mobile charges in the semiconductor channel. Conductivity maxima were observed in the transfer characteristics of all three polymer semiconductors with the LiTFSI-based electrolyte, extending the generality of this high charge carrier density-related phenomenon. Bias stress measurements on PEO/LiTFSI bottom contact OFETs indicated that the polymer semiconductors could sustain significant source−drain currents for an extended period of time (>10 min) without large drops in conductance, especially in the case of PQT-12. Further experiments are underway to optimize the polymer electrolyte composition for faster switching.

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